IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

OPTi Inc.	)	
	)	
Plaintiff,	)	
v.	)	Civil Action No. 2:07CV021(TJW)
	)	
Apple, Inc.	)	
	)	
Defendant.	)	

CLAIM CONSTRUCTION ORDER

This case came before the Court on November 26, 2008 for hearing on all claim construction issues pursuant to the Docket Control Order in this matter. The Court has reviewed the briefs of the parties and the argument had in open Court. Having carefully considered the parties arguments, the language of the claims in light of the specification and the pertinent portions of the prosecution history, and having evaluated the disputed claim terms in light of the principles of claim announced by the Federal Circuit, particularly as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*), the Court rules as set forth below as to the claim terms in dispute between the parties and enters as its order the claim constructions agreed to by the parties.

U.S. Patent 5,710,906 Claim 9	Term/Element for Construction	Court's Construction	Agreed Construction
[9.1] A method for transferring data between a bus master and a plurality of memory locations at respective addresses in an address space of a secondary memory, for use with a host processing unit and a first	**"first cache memory"**	[AGREED]	the first level of cache memory, commonly referred to as L1 cache memory.
	"said first cache memory"	[AGREED]	*See* "first cache memory"
	"secondary	[AGREED]	memory located

U.S. Patent 5,710,906 Claim 9	Term/Element for Construction	Court's Construction	Agreed Construction
cache memory which caches memory locations of said secondary memory for said host processing unit, said first cache memory having a line size of L bytes, comprising the steps of:	**memory"**		logically behind the first level cache memory, i.e., DRAM memory and, if present, L2 and L3 cache memory.
	"bus master"	[AGREED]	An I/O-bus device that initiates a data transfer on an I/O bus
[9.2] sequentially transferring at least three data units between said bus master and said secondary memory beginning at a first starting memory location address in said secondary memory address space and continuing sequentially beyond an L-byte boundary of said secondary memory address space; and	**"sequentially transferring at least three data units between said bus master and said secondary memory"**	[AGREED]	moving at least three data units between the bus master and the secondary memory in the sequence in which they are stored.
	"said bus master"	[AGREED]	*See* Limitation 9.1.
[9.3] prior to completion of the transfer of the first data unit beyond said L-byte boundary, determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said N+1'th L-byte line being the line of said secondary memory which includes said first data unit beyond said L-byte boundary,	**"prior to the completion of the transfer of the first data unit beyond said L-byte boundary"**	[AGREED]	prior to completion of the transfer of the first data unit beyond said L-byte boundary.
	"determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory"	[AGREED]	determining whether the N+1th line of data in the first cache memory is different from the corresponding data in secondary memory
[9.4] all of said transfers of data units in said step of sequentially transferring, occurring at a constant rate.	**"said transfers of data units in said step of sequentially transferring"**	[AGREED]	*See* Limitation 9.2 "sequentially transferring at least three data units between said bus master and said secondary memory."

U.S. Patent 5,710,906 Claim 9	Term/Element for Construction	Court's Construction	Agreed Construction
	"constant rate"	[AGREED]	A uniform rate
	"all of said transfers of data units"	[AGREED]	Each and every one of the at least three transfers of data units

U.S. Patent No. 6,405,291 Claim 73	Term/Element for Construction	Court's Construction	Agreed Construction
[73.1] A method for transferring a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a host processing unit and a cache memory which caches memory locations of said secondary memory for said host processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, comprising the steps of:	**"secondary memory"**	[AGREED]	*See* '906 Patent, Limitation 9.1
	"bus master"	[AGREED]	*See* '906 Patent, Limitation 9.1
	"said bus master"	[AGREED]	*See* '906 Patent, Limitation 9.1
[73.2] sequentially transferring data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first and second L-byte boundaries of said secondary memory	**"sequentially transferring data units to said bus master from said secondary memory"**	[AGREED]	moving data units to the bus master from the secondary memory in the sequence in which they are stored
	"said bus master"	[AGREED]	*See* '906 Patent, Limitation 1.1

U.S. Patent No. 6,405,291 Claim 73	Term/Element for Construction	Court's Construction	Agreed Construction
address space, each L-byte line of said transaction requiring at least 8 data unit transfers to said bus master; and			
[73.3] during the transfer of the data units for each entire N'th L-byte line in said step of transferring, initiating one and only one snoop access of said cache memory, said snoop accesses each specifying the respective N+1'th L-byte line and being initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line,	**"during the transfer of the data units for each entire N'th L-byte line"**	[AGREED]	while the data units for each entire N'th L-byte line are moving to the bus master from the secondary memory
	"the transfer of the data units"	[AGREED]	*See* Limitation 73.2 "sequentially transferring data units to said bus master from said secondary memory."
	"N+1'th L-byte line"	[AGREED]	the next sequential line following line N
	"initiating one and only one snoop access of said cache memory"	initiating one and only one next-line inquiry of said cache memory	
	"snoop access"	Next-line inquiry	
[73.4] wherein said step of transferring comprises the step of transferring to said bus master three sequential data units including the last data unit before said first L-byte boundary and the first data unit beyond said first L-byte line, all at a **constant rate**,	**"said step of transferring"**	[AGREED]	*See* Limitation 73.2 "sequentially transferring data units to said bus master from said secondary memory."
	"constant rate"	[AGREED]	A uniform rate
[73.5] and wherein said step of transferring further comprises the step of	**"said step of transferring"**	[AGREED]	*See* Limitation 73.2 "sequentially transferring data

U.S. Patent No. 6,405,291 Claim 73	Term/Element for Construction	Court's Construction	Agreed Construction
transferring to said bus master three sequential data units including the last data unit before said second L-byte boundary and the first data unit beyond said second L-byte line, all at a constant rate.			units to said bus master from said secondary memory."

U.S. Patent No. 6,405,291 Claim 74	Term/Element for Construction	Court's Construction	Agreed Construction
[74.1] A method according to claim 73, wherein said step of sequentially transferring data units continues further beyond a third L-byte boundary of said secondary memory, and wherein said step of transferring further comprises the step of transferring three sequential data units including the last data unit before said third L-byte boundary and the first data unit beyond said third L-byte line, all at a constant rate.	**"said step of sequentially transferring data units"**	[AGREED]	*See* Limitation 73.2 "sequentially transferring data units to said bus master from said secondary memory."
	"said step of transferring"	[AGREED]	*See* Limitation 73.2 "sequentially transferring data units to said bus master from said secondary memory."
	"constant rate"	[AGREED]	*See* Limitation 73.4

U.S. Patent No. 6,405,291 Claim 88	Term/Element for Construction	Court's Construction	Agreed Construction
[88.1] Controller apparatus for a computer system which includes a secondary memory having an address space, a bus master, a host processing unit and a cache memory which caches memory locations of said secondary memory for said host processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in response to a PCI-bus burst read transaction initiated by said bus master,	**"cache memory"**	[AGREED]	*See* Limitation 73.1
	"secondary memory"	[AGREED]	*See* '906 Patent, Limitation 9.1
	"said cache memory"	[AGREED]	*See* Limitation 73.1
	"bus master"	[AGREED]	*See* '906 Patent, Limitation 9.1.
	"said bus master"	[AGREED]	*See* '906 Patent, Limitation 9.1.
[88.2] sequentially transfers data units to said bus master from said secondary memory according to said PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first, second and third L-byte boundaries of said secondary memory address space, each full L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, a plurality of sequential data units bracketing at least said first, second and third L-byte boundaries being transferred to said bus master at a constant rate, said constant rate being dependent upon the frequency of a PCI-bus clock provided to said bus master; and	**"sequentially transfers data units to said bus master from said secondary memory"**	[AGREED]	moving data units to the bus master from the secondary memory in the sequence in which they are stored
	"constant rate"	[AGREED]	*See* '906 Patent, Limitation 9.4
	"at a constant rate"	[AGREED]	*See* '906 Patent, Limitation 9.4
	"sequentially transfers data units to said bus master from said secondary memory according to said PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond	[AGREED]	This is not a means-plus-function element and, therefore, it need not be construed according to 35 U.S.C. §112 ¶ 6.

U.S. Patent No. 6,405,291 Claim 88	Term/Element for Construction	Court's Construction	Agreed Construction
	at least first, second and third L-byte boundaries of said secondary memory address space, each full L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, a plurality of sequential data units bracketing at least said first, second and third L-byte boundaries being transferred to said bus master at a constant rate, said constant rate being dependent upon the frequency of a PCI-bus clock provided to said bus master"		

SIGNED this 4th day of December, 2008.

CHARLES EVERINGHAM IV
UNITED STATES MAGISTRATE JUDGE